

# NTMS4107N

## Power MOSFET

30 V, 18 A, Single N-Channel, SO-8

### Features

- Ultra Low  $R_{DS(on)}$  (at 4.5 V<sub>GS</sub>), Low Gate Resistance and Low Q<sub>G</sub>
- Optimized for Low Side Synchronous Applications
- High Speed Switching Capability
- Pb-Free Package is Available

### Applications

- Notebook Computer Vcore Applications
- Network Applications
- DC-DC Converters

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating		Symbol	Value	Unit
Drain-to-Source Voltage		V <sub>DSS</sub>	30	V
Gate-to-Source Voltage		V <sub>GS</sub>	±20	V
Continuous Drain Current (Note 1)	Steady State	T <sub>A</sub> = 25°C	15	A
		T <sub>A</sub> = 85°C	11	
	t ≤ 10 s	T <sub>A</sub> = 25°C	18	
Power Dissipation (Note 1)	Steady State	T <sub>A</sub> = 25°C	1.67	W
		t ≤ 10 s	2.5	
Continuous Drain Current (Note 2)	Steady State	T <sub>A</sub> = 25°C	11	A
		T <sub>A</sub> = 85°C	8.0	
		T <sub>A</sub> = 25°C	0.93	
Power Dissipation (Note 2)		P <sub>D</sub>	0.93	W
Pulsed Drain Current	t <sub>p</sub> = 10 μs	I <sub>DM</sub>	56	A
Operating Junction and Storage Temperature		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Continuous Source Current (Body Diode)		I <sub>S</sub>	3.0	A
Single Pulse Drain-to-Source Avalanche Energy (V <sub>DD</sub> = 30 V, V <sub>GS</sub> = 10 V, I <sub>PK</sub> = 32 A, L = 1 mH, R <sub>G</sub> = 25 Ω)		E <sub>AS</sub>	512	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T <sub>L</sub>	260	°C

### THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	R <sub>θJA</sub>	75	°C/W
Junction-to-Ambient - t ≤ 10 s (Note 1)	R <sub>θJA</sub>	50	
Junction-to-Ambient - Steady State (Note 2)	R <sub>θJA</sub>	135	

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

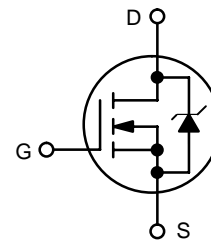
1. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [1 oz] including traces).
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.412" sq.).



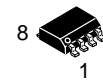
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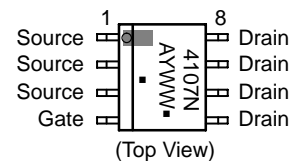
V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> TYP	I <sub>D</sub> MAX
30 V	3.4 mΩ @ 10 V	18 A
	4.7 mΩ @ 4.5 V	



### MARKING DIAGRAM/ PIN ASSIGNMENT



SO-8  
CASE 751  
STYLE 12



4107N = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ■ = Pb-Free Package  
 (Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NTMS4107NR2	SO-8	2500/Tape & Reel
NTMS4107NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			21		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.0		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			7.4		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 14\text{ A}$		4.7	5.5	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		3.4	4.5	
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 18\text{ A}$		25		S

## CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		6000		pF
Output Capacitance	$C_{OSS}$			1030		
Reverse Transfer Capacitance	$C_{RSS}$			550		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 18\text{ A}$		45		nC
Threshold Gate Charge	$Q_{G(TH)}$			6.5		
Gate-to-Source Charge	$Q_{GS}$			16.3		
Gate-to-Drain Charge	$Q_{GD}$			19.3		
Gate Resistance	$R_G$			0.60		

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 1.0\text{ A}, R_G = 6.0\ \Omega$		9.0		ns
Rise Time	$t_r$			10		
Turn-Off Delay Time	$t_{d(OFF)}$			94		
Fall Time	$t_f$			38		

## DRAIN-SOURCE DIODE CHARACTERISTICS

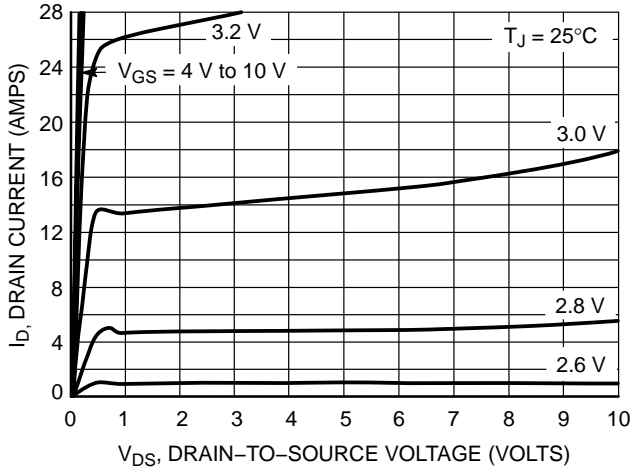
Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 3.0\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.1	V
			$T_J = 125^\circ\text{C}$		0.6		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 3.0\text{ A}$		41		ns	
Charge Time	$t_a$			20			
Discharge Time	$t_b$			21			
Reverse Recovery Charge	$Q_{RR}$			48			nC

3. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

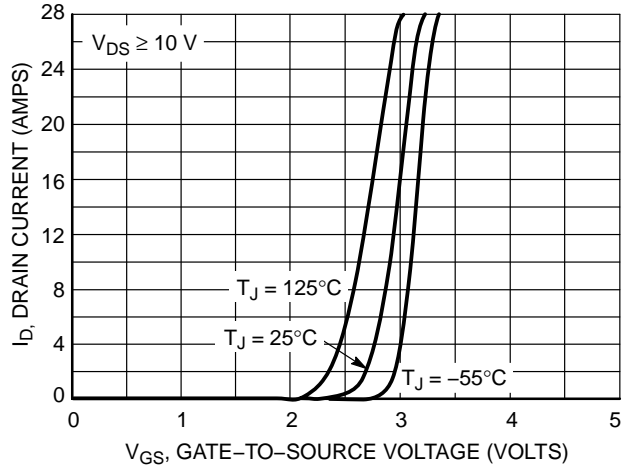
4. Switching characteristics are independent of operating junction temperatures.

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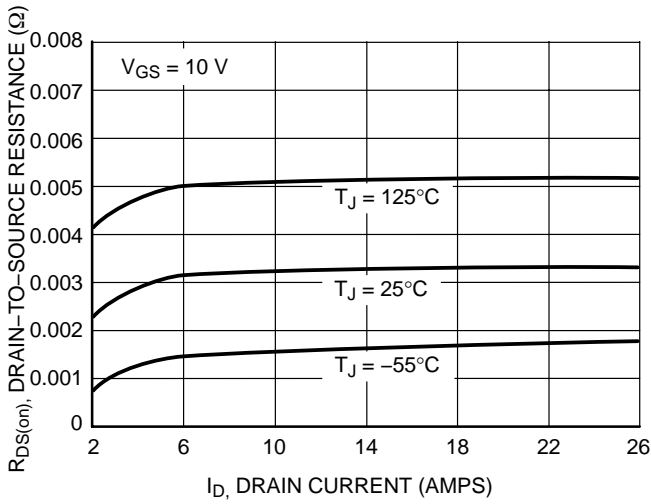
## TYPICAL PERFORMANCE CURVES



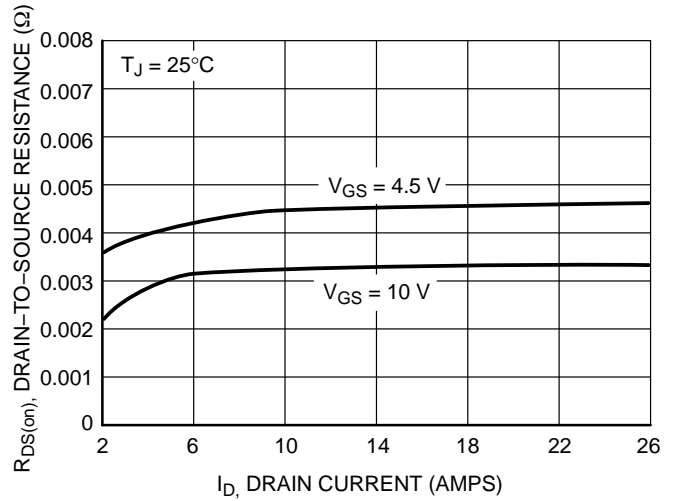
**Figure 1. On-Region Characteristics**



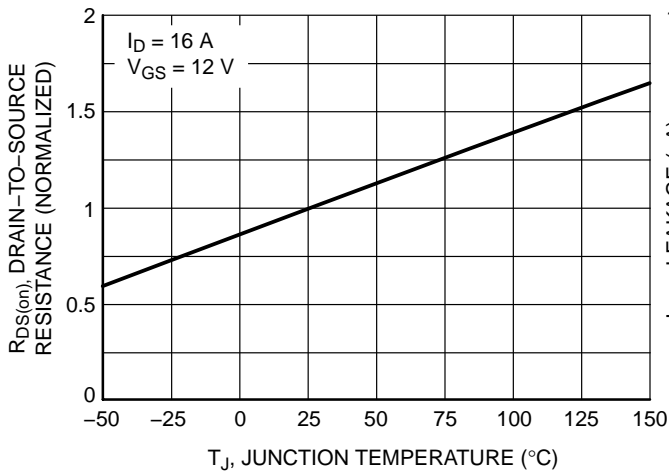
**Figure 2. Transfer Characteristics**



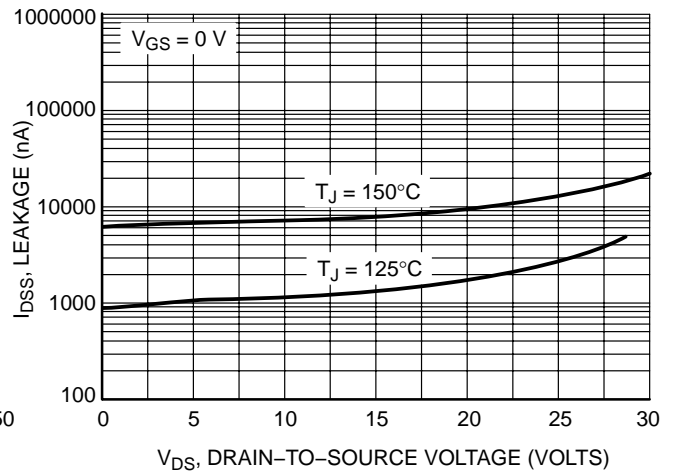
**Figure 3. On-Resistance vs. Drain Current and Temperature**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

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## TYPICAL PERFORMANCE CURVES

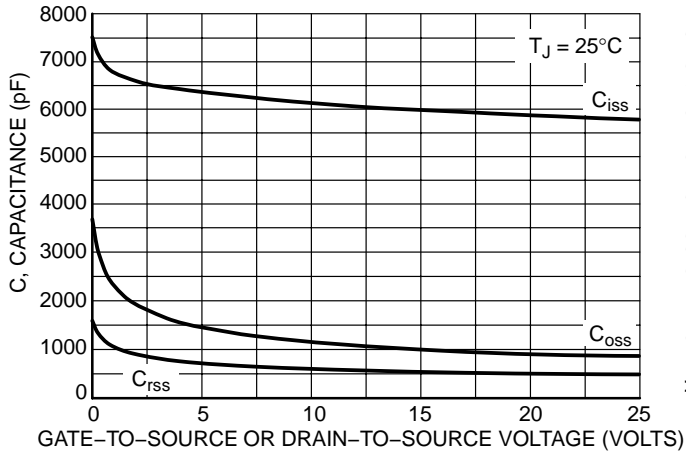


Figure 7. Capacitance Variation

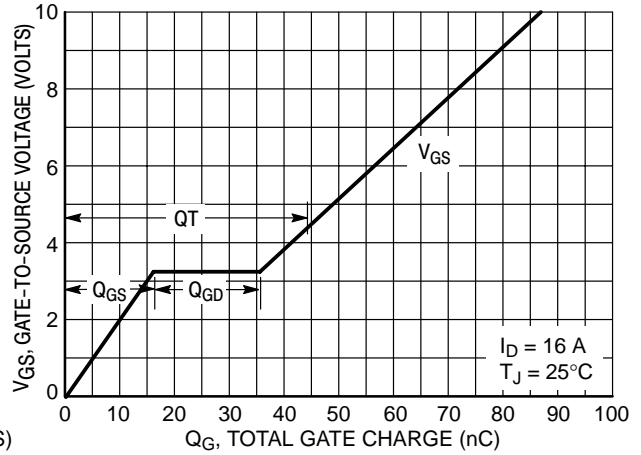


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

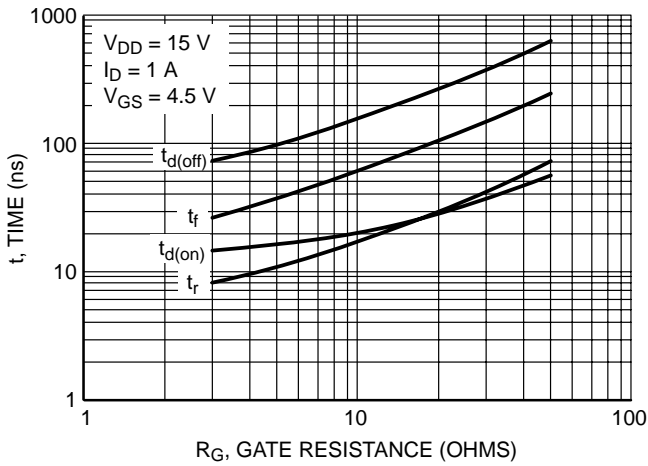


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

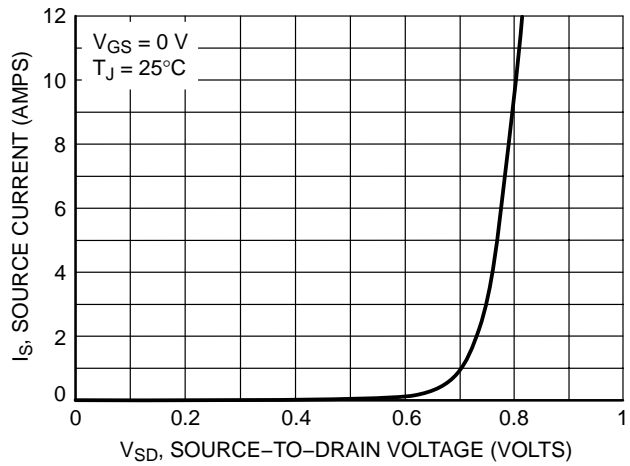


Figure 10. Diode Forward Voltage vs. Current

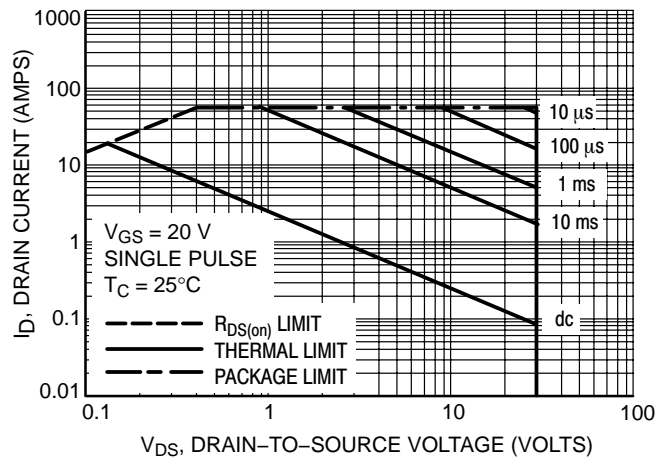
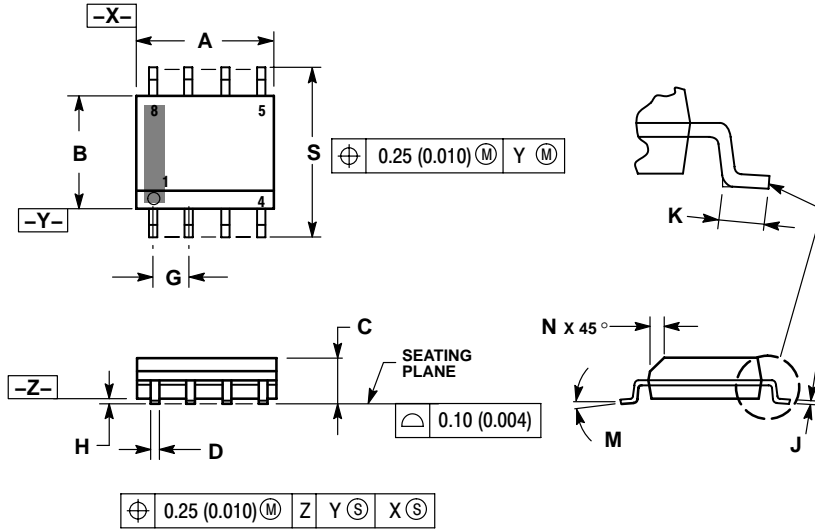


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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## PACKAGE DIMENSIONS

SO-8  
CASE 751-07  
ISSUE AG



### NOTES:

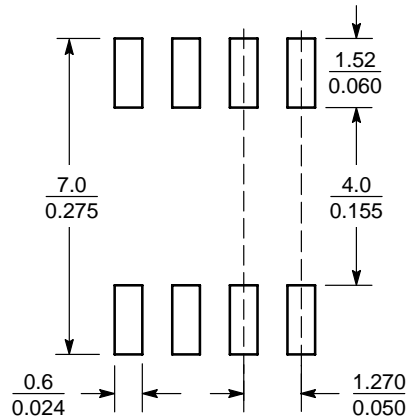
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### STYLE 12:

- PIN 1: SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN  
6. DRAIN  
7. DRAIN  
8. DRAIN


### SOLDERING FOOTPRINT\*



SCALE 6:1 ( $\frac{\text{mm}}{\text{inches}}$ )

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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